*Replace the paragraph beginning at page 4, line 25, with:*

Secondly, by patterning the signal interconnections 108a and 126a under the first Al interconnection layer 129, a difference in an interlayer thickness under the first Al interconnection layer 129 occurs between a portion having a signal pattern and a portion not having a signal pattern, stray capacitance to the base fluctuates, and a difference occurs between actual resistance and the simulated resistance during circuit design (see Fig. 14). The fluctuation in stray capacitance becomes a serious problem in the pattern in which a change of the signal interconnection or the like is not desirable. Further, during operation of the semiconductor device, the signal interconnection is electrically affected by the pattern of other signal interconnection on the upper layer or the lower layer. Therefore, stable signal circuit cannot be obtained.

*IN THE CLAIMS*

*Replace the indicated claims with:*

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a plurality of regions;

a resistor group including a plurality of resistors located in one of said regions of said semiconductor substrate;

a metal interconnection layer opposite the region in which said resistor group is located; and

a shielding layer between said resistor group and said metal interconnection layer.

2. (Amended) The semiconductor device according to claim 1, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

3. (Amended) The semiconductor device according to claim 1, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

4. (Amended) The semiconductor device according to claim 1, wherein said shielding layer has a fixed potential.

5. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a signal interconnection layer on said semiconductor substrate; and

a shielding layer on at least one side of said signal interconnection layer.

6. (Amended) The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a gate electrode layer in said DRAM region and used as said shielding layer in said logic region.

7. (Amended) The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

8. (Amended) The semiconductor device according to claim 5, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

9. (Amended) The semiconductor device according to claim 5, wherein said shielding layer has a fixed potential.

10. (Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a shielding layer in said DRAM region and said logic region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

12. (Amended) The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is said shielding layer.

13. (Amended) The method according to claim 10, further comprising fixing potential of said shielding layer.

14. (Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a signal interconnection layer in said logic region; and

forming a shielding layer on at least one side of said signal interconnection layer in said DRAM region and said logic region.

17. (Amended) The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is said shielding layer.

18. (Amended) The method according to claim 14, further comprising fixing potential of said shielding layer.

*IN THE ABSTRACT*

*Replace the abstract with:*

ABSTRACT OF THE DISCLOSURE

A semiconductor device has a semiconductor substrate and a resistor group and/or a signal interconnection layer in a region of the semiconductor substrate. A shielding layer is located above and/or below the region where the resistor group and/or the signal interconnection layer are located.

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